In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 5, 6, 8, 13-16, and 21-26.

1. (Currently Amended) An apparatus, comprising:

an integrated circuit including:

a first processor with a first dedicated cache;

a second processor with a second dedicated cache; and

control logic, coupled to the first and second dedicated caches, having: ~~to receive a first cache line directly from the first dedicated cache and to transfer the first cache line directly to the second dedicated cache.~~

a first multiplexer coupled to the first and second caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache; and

a second multiplexer coupled to the first and second caches to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache.

2. (Previously Presented) The apparatus of claim 1, wherein:

the control logic is to transfer the first cache line if the first cache line is a cache line in the first dedicated cache and not in the second dedicated cache.

3. (Previously Presented) The apparatus of claim 1, wherein:

the control logic is to transfer the first cache line if the first cache line is a modified version of a particular cache line and the second dedicated cache contains an unmodified version of the particular cache line.

4. (Original) The apparatus of claim 1, further comprising:

a coherency unit to perform snoop operations on the first and second dedicated caches.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) The apparatus of claim 1, wherein the integrated circuit further includes:

a shared cache coupled to the control logic, to the first dedicated cache, and to the second dedicated cache;

wherein the control logic is further to transfer a second cache line from the second dedicated cache to the first dedicated cache;

wherein the control logic includes a first write buffer to receive the first cache line from the first dedicated cache and to provide the first cache line to the shared cache, and further includes a second write buffer to receive the second cache line from the second dedicated cache and provide the second cache line to the shared cache;

wherein the shared cache is to provide the first cache line to the second dedicated cache and to provide the second cache line to the first dedicated cache.

8. (Cancelled)

9. (Currently Amended) ~~The apparatus of claim 1, wherein:~~

An apparatus, comprising:

an integrated circuit including:

a first processor with a first dedicated cache;

a second processor with a second dedicated cache; and

control logic, coupled to the first and second dedicated caches, having:

a first fill buffer coupled to the first and second dedicated caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache; and

~~the control logic includes~~ a second fill buffer coupled to the first and second dedicated caches to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache.

10. (Currently Amended) The apparatus of claim 9 ~~1~~, further comprising ~~wherein the control logic includes~~:

~~a multiplexer coupled to the first and second caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache.~~

a coherency unit to perform snoop operations on the first and second dedicated caches.

11. (Currently Amended) The apparatus of claim 9 ~~1~~, wherein the integrated circuit further ~~control logic~~ includes:

~~a first multiplexer coupled to the first and second caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache; and~~

~~a second multiplexer coupled to the first and second caches to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache.~~

a shared cache coupled to the control logic, to the first dedicated cache, and to the second dedicated cache;

wherein the control logic is further to transfer a second cache line from the second dedicated cache to the first dedicated cache;

wherein the control logic includes a first write buffer to receive the first cache line from the first dedicated cache and to provide the first cache line to the shared cache, and further includes a second write buffer to receive the second cache line from the second dedicated cache and provide the second cache line to the shared cache;

wherein the shared cache is to provide the first cache line to the second dedicated cache and to provide the second cache line to the first dedicated cache.

12. (Currently Amended) A method, comprising:

transferring a first cache line directly from a first dedicated cache of a chip multi-processor to a first multiplexer within control logic coupled to the first cache in the chip multi-processor; ~~and~~

subsequently transferring the first cache line from the ~~control logic~~ first multiplexer directly to a second dedicated cache of the chip multi-processor.

transferring a second cache line directly from the second dedicated cache to a second multiplexer within the control logic coupled to the second cache in the chip multi-processor; and

subsequently transferring the second cache line from the second multiplexer directly to the first dedicated cache.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Currently Amended) ~~The method of claim 12, wherein:~~

~~the transferring the first cache line from the first dedicated cache includes transferring the first cache line from the first dedicated cache to a multiplexer; and~~

~~the transferring the first cache line from the control logic includes transferring the first cache line from the multiplexer to the second dedicated cache.~~

A method, comprising:

transferring a first cache line directly from a first dedicated cache of a chip multi-processor to a first write buffer within control logic coupled to the first cache in the chip multi-processor;

subsequently transferring the first cache line from the first write buffer directly to a second dedicated cache of the chip multi-processor.

transferring a second cache line directly from the second dedicated cache to a second write buffer within the control logic coupled to the second cache in the chip multi-processor; and

subsequently transferring the second cache line from the second write buffer directly to the first dedicated cache.

18. (Currently Amended) A system, comprising:

a main memory,

a chip multiprocessor coupled to the main memory and including:

a first processor with a first dedicated cache;

a second processor with a second dedicated cache; and

control logic, coupled to the first and second dedicated caches, having: ~~to receive a first cache line directly from the first dedicated cache and to transfer the first cache line directly to the second dedicated cache.~~

a first multiplexer coupled to the first and second caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache; and

a second multiplexer coupled to the first and second caches to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache.

19. (Currently Amended) The system of claim 18, wherein the chip multiprocessor further comprises:

~~the control logic is further to a transfer second cache line from the second dedicated cache to the first dedicated cache entirely within the chip multiprocessor.~~

a coherency unit to perform snoop operations on the first and second dedicated caches.

20. (Previously Presented) The system of claim 18, wherein the chip multiprocessor further includes:

a shared cache coupled to the control logic and to the second dedicated cache to provide the first cache line to the second dedicated cache;

wherein the control logic includes a write buffer to receive the first cache line from the first dedicated cache and to provide the first cache line to the shared cache.

21-26. (Cancelled)